Remarks

Reconsideration of this application is requested. Claims 1, 3, 8, 12, 15, 16, 17 and 21 have been amended. Claims 13, 14, 19, 22 and 23 have been withdrawn. Claims 1-12, 15-18 and 20-21 remain in the application.

Drawings

Applicants will submit formal drawings once a Notice of Allowance has been received.

Claim 8

The Office Action states that claim 8 is objected and needs appropriate correction. By this amendment claim 8 has been modified and is believe to overcome the objection.

Response to the 35 U.S.C. §102 (e) Rejection

The Office Action rejects claims 1-3, 7-18 and 20-23 under 35 U.S.C. §102(e) as being anticipated by Arimoto (US. 6,256,252 B1).

Claims 1-3 and 7-11

The prior art reference of Arimoto shows in FIG. 1 an operating potential of VDDL being supplied for a logic circuit 2 and another operating potential of VDDM being supplied for a memory circuit 3. Arimoto states in column 4, lines 29-41, that a sleep mode instruction signal SLP causes data in logic circuit 2 to be saved in memory circuit 3. Once data has been transferred from logic circuit 2 to memory circuit 3 and saved, the main processor stops supplying the operating potential VDDL to the logic circuit. The main processor supplies the operating potential VDDM to the memory circuit regardless of the active state of the sleep mode instruction signal SLP. Thus, Arimoto teaches that the main processor supplies two separate operating potentials, one VDDL potential to the logic circuit and one VDDM to the memory circuit.

Applicants' amended claim 1 recites, among other things, a second circuit coupled to receive a power supply potential from the first circuit in a first operational mode and decoupled from receiving the power supply potential when the first circuit is

not in the first operational mode. Support for the amended language of Applicants' claim 1 is illustrated in FIGs. 2 and 3 that shows logic circuit 220 coupled to receive an operating potential from memory circuit 210 when enabled (signal ACTIVE) and decoupled when not enabled. Thus, Applicants' claim 1 states that the power supply potential for the second circuit is supplied from the first circuit, which is in contrast to Arimoto that teaches the main processor supplies separate power supply potentials to both the first and second circuits.

Accordingly, the relied upon prior art of Arimoto cannot anticipate Applicants' amended claim 1. Claims 2-3 and 7-11 depend, either directly or indirectly from base claim 1, and are believed to be allowable over the art of record for at least the same reasons as claim 1.

Claims 12-16

Applicants' amended claim 12 recites, among other things, supplying a power supply voltage potential to a memory circuit and coupling the power supply voltage potential from the memory circuit to a logic circuit.

Again, it is respectfully pointed out that Arimoto supplies one power supply voltage potential to the memory circuit and another power supply voltage potential to the logic circuit. In contrast, Applicants' claim one power supply voltage potential supplied to a memory circuit that is coupled to the logic circuit. Accordingly, the relied upon prior art of Arimoto cannot anticipate Applicants' amended claim 12. Claims 13 and 14 have been withdrawn by this amendment. Claims 15-16 depend from base claim 12 and are believed to be allowable over the art of record for at least the same reasons as claim 12.

Claims 17-18 and 20-23

Applicants' claim 17 recites, among other things, a first circuit to receive a power supply potential and a second circuit coupled to the first circuit to receive the power supply potential in a first operational mode.

As previously mentioned Arimoto teaches a main processor supplying one power supply voltage potential to memory circuit and a second power supply voltage potential to logic circuit. Arimoto separates the power supply conductors in the memory circuit

from the logic circuit and uses the main processor to supply both. On the other hand, Applicants claim one power supply potential supplied to a first circuit and a second circuit coupled to the first circuit to receive the power supply potential in a first operational mode. Accordingly, the relied upon prior art of Arimoto cannot anticipate Applicants' amended claim 17. Claims 18 and 20-21 depend, either directly or indirectly, from base claim 17 and are believed to be allowable over the art of record for at least the same reasons as claim 17. Claims 22 and 23 have been withdrawn by this amendment.

Response to the 35 U.S.C. §103 (a) Rejection

The Office Action rejects claims 4-6 and 19 under 35 U.S.C. §103(a) as being unpatentable over Arimoto in U.S. Patent No. 6,256,252.

Claims 4-6 depend from amended claim 1 and claim 19 depends from amended claim 17. Applicants' believe that base claims 1 and 17 have been amended to include features not found in the art of record. In particular, the feature of supplying a power supply voltage potential to the memory circuit and coupling that potential to the logic circuit is not found in Arimoto. Therefore, Applicants' believe that the rejection of claims 4-6 and 19 has been overcome.

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Conclusion

The foregoing is submitted as a full and complete response to the Office Action mailed December 16, 2003, and it is submitted that claims 1-12, 15-18 and 20-21 are in condition for allowance. Reconsideration of the rejection of claims is requested and the allowance of claims 1-12, 15-18 and 20-21 is earnestly solicited.

Should it be determined that a fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #50-0221.

If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (480) 552-1388 is respectfully solicited.

Respectfully submitted,
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